POSEIDON
Design Systems

SDR Test Signal Generator
Release 2.0

SDR-TSG is an FPGA based communication signal emulator optimized for Xilinx FPGAs. This tool allows the user to generate different type of complex communication signals added with practical noise inside the FPGA. The modulation capabilities include both analog and digital modulation schemes. User can control the signals to be generated in FPGA using GUI running on PC. The communication between PC and FPGA is realized with low weight UART core.

SDR-TSG is bundled with the GUI software module, FPGA core and one hardware module, which are described below.

- ♦ Signal profile creator GUI application software running on Windows based PC
  - o JAVA based user friendly GUI
  - o Options to create signals with specific characteristics and profiles with group of signals
  - o Generates functional level equivalent OCTAVE/MATLAB files
- ♦ Synthesized cores and wrapper VHDL files for Xilinx FPGAs
  - o Xilinx synthesized netlist for all families of FPGAs
  - o Wrapper VHDL files and example codes
- ♦ Universal UART dongle hardware module
  - o Can be connected to any Xilinx FPGA board
  - o Comes with 6 pin male connecter

The software on PC allows the user to set the profile with several signals each with any complex communication technique. Each signal parameters such as modulation, carrier frequency and type of signal can be selected. The profile once communicated to core in FPGA it produces the signals and combines them as per the predefined settings. The core also provides options to add noise to   signal emulating the situation of practical ADC output coming into FPGA.

- □ Types of signals
   Fixed carrier, FHSS, DSSS, Burst

- □ Types of analog modulations
   AM-DSBSC, AM-DSBFC, AM-SSB,FM

- □ Types of digital modulations
   ASK, BPSK, BFSK, M-PSK, 16-QAM, 64-QAM

- □ Carrier parameters for each signal
   Frequency, power

- □ Modulating signal options
   Random signal generated within FPGA, from a file on PC, user entered data from PC

- □ Function generator options
   SIN, square, Triangular, any random shape specified through samples.

- □ Noise options
   AWGN with specific power levels

- □ licensing options : (a) Synthesized netlists and wrapper VHDL   (ordering code: SDR-TSG-02-SYN)
                     (b) Full VHDL source code (ordering code: SDR-TSG-02-HDL)

For more information email us at info@poseidon-systems.com

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