Triton Tuner™ - *Xilinx FPGA Systems*

POSEIDON
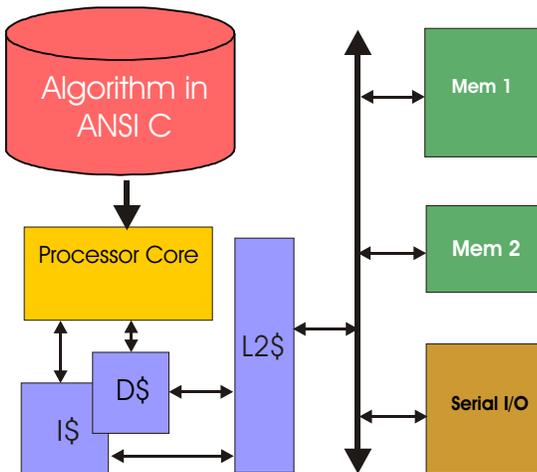Design Systems

System Design Environment

The Triton Tuner is a system level design environment which enables designers to quickly analyze their architecture and modify their system for optimal performance. The tool is optimized for Audio, Video, VoIP, Imaging, wireless, storage and security applications.

Most systems consist of processors, caches, memories, buses, peripherals, function blocks, and software algorithms. It is critical for the architecture to support the efficient flow of data between the blocks to meet the performance requirements of the system. The Triton Tuner environment provides the capabilities critical to the designer for developing a robust and efficient solution. Tuner utilizes a SystemC simulation environment based on transaction level models of the system components. The hardware/software cosimulation enables the tool to collect key system performance measurements. These
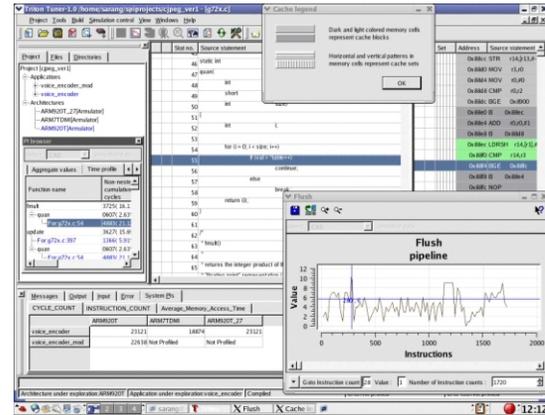
Triton Tuner corelating pipeline flushes
with source code for rapid software optimization

measurements identify the bottlenecks in the architecture which are limiting performance. Tuner provides a user friendly interface and data visualization browser to greatly increase the efficiency of the design effort. Tuner also performs software profiling as well as the collection of system performance indices. These measurements pinpoint inefficiencies in the design and enable the concurrent optimization of the system architecture and the software. Triton Tuner also models the complete memory hierarchy which includes cache memories, write buffers, busses, RAMs, flash memories, etc. With the key performance and utilization data available for the different components of the memory subsystem, you can quickly configure the memory subsystem to achieve maximum performance with lower power consumption.

Typical system which can
be optimized with Triton

Key Functions of Tuner

Increase system performance by creating an efficient memory hierarchy

Optimize system performance to create designs with lower power dissipation

Tune software algorithms to run faster with less hardware inefficiencies

Reduce system optimization effort by using an effective and user friendly system analysis environment

Identify hot spots in algorithms through detailed profiling and reduce power by optimizing critical code

Identify and eliminate bottlenecks between the hardware and the software

Features	Benefits
Application profile plus memory usage data	Easily tune application code and memory hierarchy
Extensive cache Performance Indices	Tune cache architecture to algorithm
Memory performance measurements	Select optimum memories - size, type, speed, and configuration
Correlation between performance data and source code	Identifies problem areas between the application code and the hardware
Software profiling and Performance Indices	Speeds system bottleneck identification, software optimization and HW/SW partitioning
User friendly data presentation and visualization	Reduction of analysis time, faster and more accurate tuning decisions
Co-verification environment based on transactional models	Fast simulation speeds
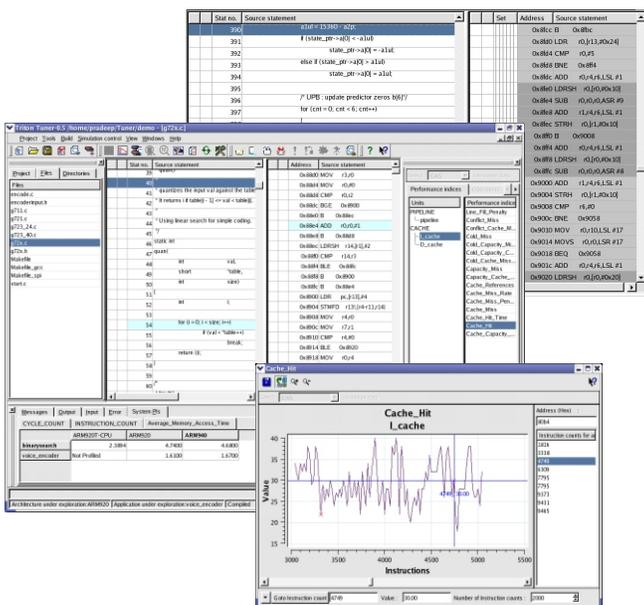
I Cashe Hit Performance Index

Easy to Identify and correct memory bottlenecks

Using Triton Tuner, bottlenecks in the system design can be identified, isolated and corrected in a easy and quick manner. This greatly facilitates the task of developing a robust architecture which meets the system performance goals. With the key data presentation and user friendly graphical user interface, the designer saves weeks of effort that it takes to develop and optimize a complex system.

Memory Models

Cache	DRAM	SRAM	FPM DRAM
Scratch Pad	EDO DRAM	Write buffer	BEDO DRAM
Mem. Contr.	SDRAM		

Processors Platforms Supported

ARM™
MicroBlaze™
PowerPC™

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